Introduction

Every HSP50110/210EVAL Evaluation Kit contains a floppy disk labeled DEMOD CHIPSET EVALUATION SOFTWARE. This disk contains the DEMODEVB.EXE file and other software necessary to configure and operate the evaluation card which is provided in the demod chipset kit. This kit provides all the software required for the configuration, operation and evaluation of the HSP50110 Digital Quadrature Tuner (DQT) and HSP50210 Digital Costas Loop (DCL). Additional software is provided to demonstrate the various filtering features of the evaluation board. The software provided in the kit ensures that a user can quickly set up the evaluation board, configure it, and output data for test evaluation. This Evaluation Kit will leave the user confident that these parts can be easily ported into an application specific design. Four directories (folders) are provided to assist in familiarizing the evaluator with key features of the chipset. These four directories are labeled "examples", "filters", "schemat" and "serinade" and are provided for this purpose.

The "EXAMPLES" Folder

The first directory is filled with example configuration files which have been tested and proven to provide BER performance that is better than 1dB from theory. **It is the use of these example configuration files that is the focus of this Application Note.** This Application Note will detail the location, use and application of the example configuration files. The quickest way to configure the Evaluation Board for your application, is to find a configuration file that most closely matches your symbol rate, and load that file. The file can then be edited to change any of the parameters (such as IF Frequency, Filtering, etc.) as needed.

Figures 1A and 1B detail the test Hardware configurations used to verify the BER performance of each configuration file. A study of these figures reveals that Figure 1A utilizes a 70MHz IF, while Figure 1B utilizes a 5MHz IF. These are the only two IF frequencies that will be found in the example files.

The "FILTERS" Folder

This folder contains example FIR filter configuration files. These files have been created with SERINADE, a software package developed for Intersil Corporation to assist in the design of digital filters of the type found on the Evaluation Board. This Application Note will provide information on the description, and use of these filter files.

The "SCHEMAT" Folder

This folder contains the Schematic of the Evaluation Board, as captured using the ORCAD Application. The files are provided for design re-use and should help shorten the critical "Time to Market" development time. These schematics, which were used to generate the Evaluation Board, are offered for use in designs, it is the user's responsibility to secure the proper ORCAD Revision and any ORCAD technical assistance in porting, opening and editing these schematics.
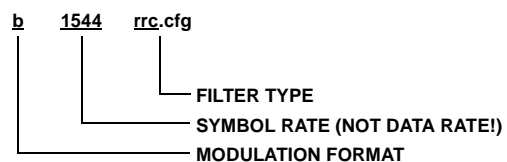
The "SERINADE" Folder

This folder contains the latest version of the SERINADE software. This software will assist in any application specific FIR filter design. The "filters" folder contains examples of filters already designed using this software, and should be used to verify results until the user is proficient with the application. All SERINADE generated filters are readily ported into a format that the HSP50110/210EVAL Kit can import.

It is highly recommended that the distribution disk provided in the evaluation kit be backed up prior to use. Obtain a printout of the files in the "EXAMPLES" and "FILTERS" and use it to maintain a fully functional software package.

The "EXAMPLE" Configuration Files

The example configuration files included on the distribution disk are labeled according to the key shown below and in Appendix H of the User's Manual. The first field is an alphanumeric digit which indicates the modulation type. Options are: B for BPSK, Q for QPSK, and E for 8PSK. In the future F will be used to denote FSK, while M will denote MSK.

<u>**b**</u>   <u>**1544**</u>   <u>**rrc**</u>.cfg

```
                        └── FILTER TYPE
                   └────── SYMBOL RATE (NOT DATA RATE!)
         └────────────── MODULATION FORMAT
```

The second field is numeric and represents the symbol, or baud rate of the signal, expressed in KHz. The symbol rate numeric field utilizes a "p" to represent a decimal point. For example, a data rate of 1200bps is represented as 1p2. Similarly 9600bps is expressed as 9p6.
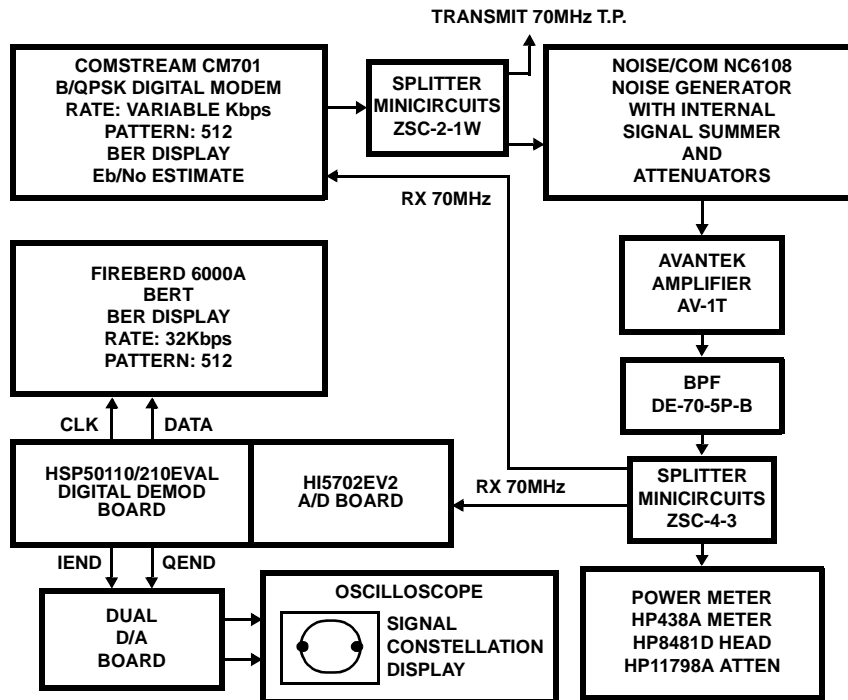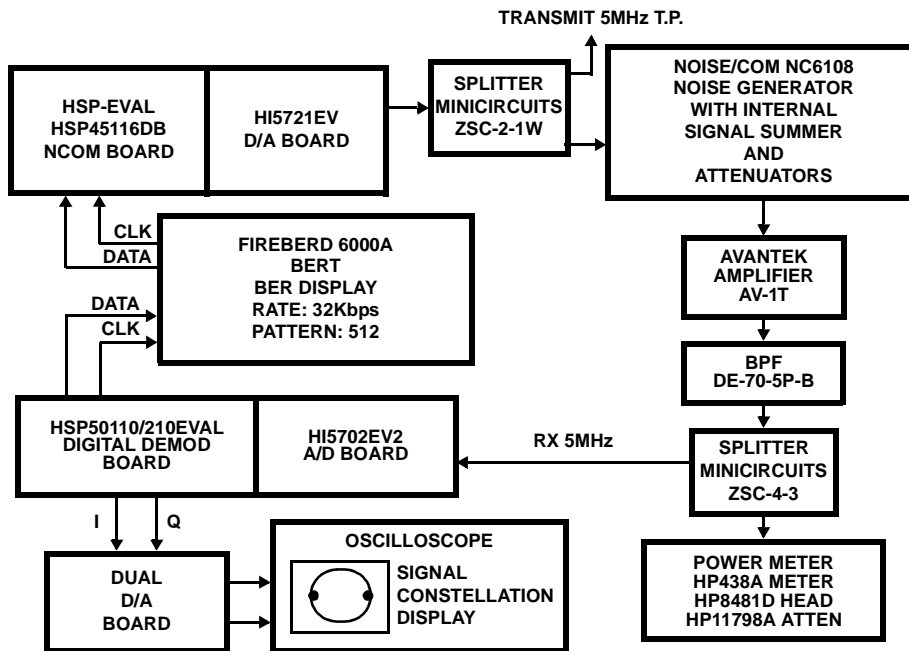
FIGURE 1A. 70MHz IF TEST CONFIGURATION

FIGURE 1B. 5MHz TEST CONFIGURATION

Care must be taken not to confuse symbol rate with data rate. Recall that for BPSK, data rate and symbol rate are identical. For QPSK, however, the symbol rate is 1/2 the data rate, because two bits of data are used to form a symbol. For 8PSK the symbol rate is 1/3 the data rate, because three bits of data are used to form a symbol. Figure 2 details how a typical QPSK modulator is implemented, while Figure 3 illustrates the data to quadrature symbol relationship for QPSK for both the in-phase and quadrature components. Two data bits will determine in which of four phase states the carrier will be placed: 0°, 90°, 180°, or 270°. This phase shift is accomplished using the I (in-phase) and (Q) quadrature orthogonal vectors as shown in Figure 4. Figure 5 illustrates the data and symbol relationship for 8PSK, while Figure 6 shows the possible carrier vectors created for a symbol.
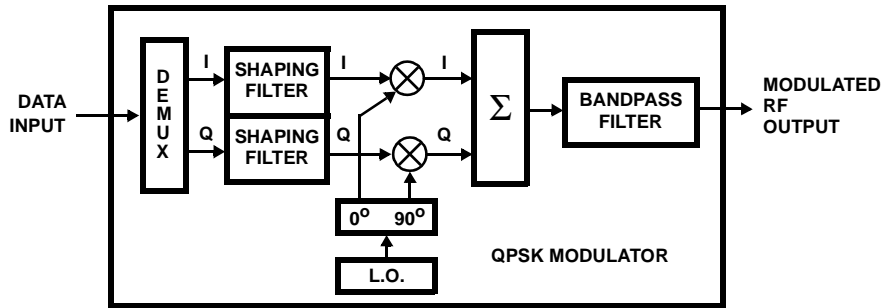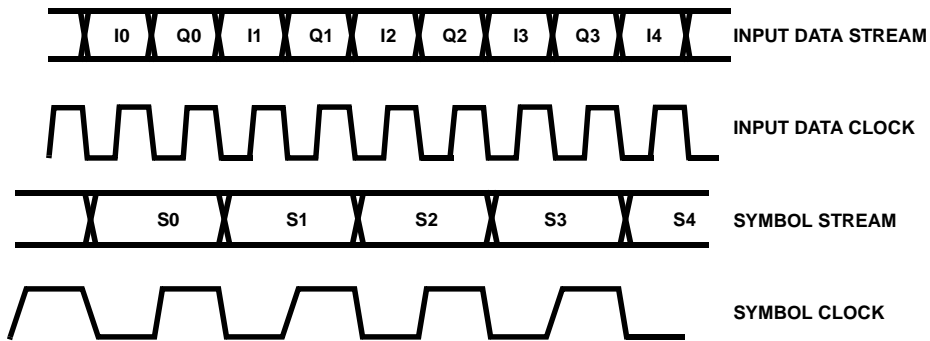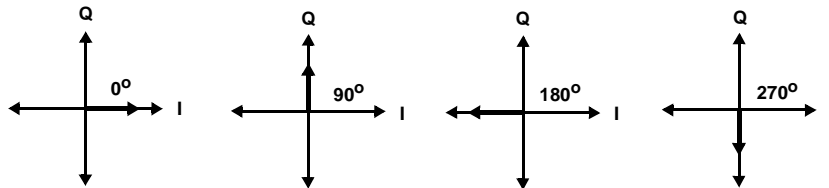
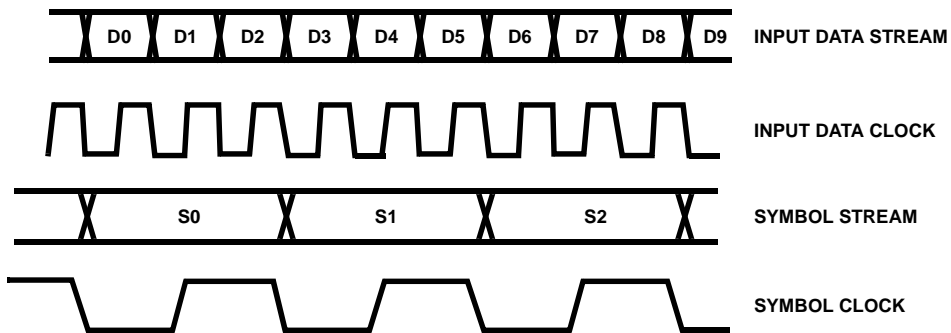**FIGURE 2.**

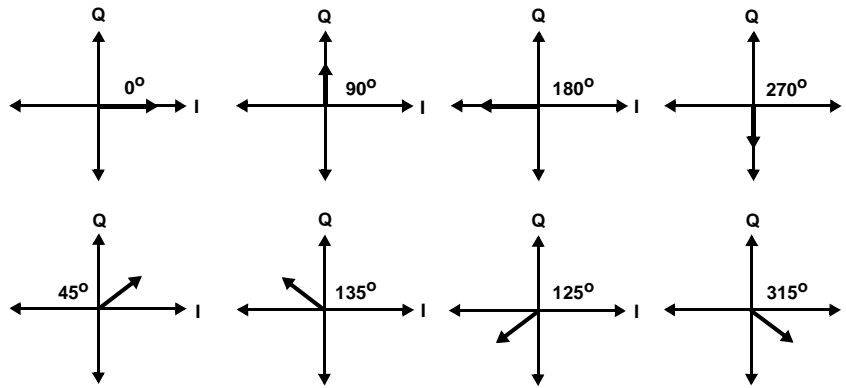**FIGURE 3.**

FIGURE 4.

FIGURE 5.

FIGURE 6. VECTOR REPRESENTATIONS OF THE 8PSK SYMBOLS CREATED FROM THREE DATA BITS
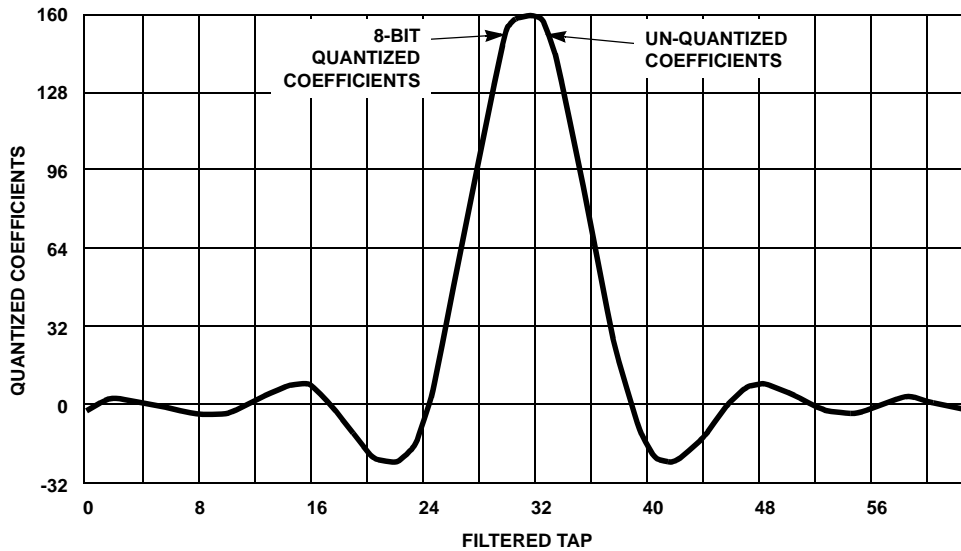

FIGURE 7. COEFFICIENTS FOR THE SQUARE ROOT OF RAISED COSINE α = 0.4FILTER
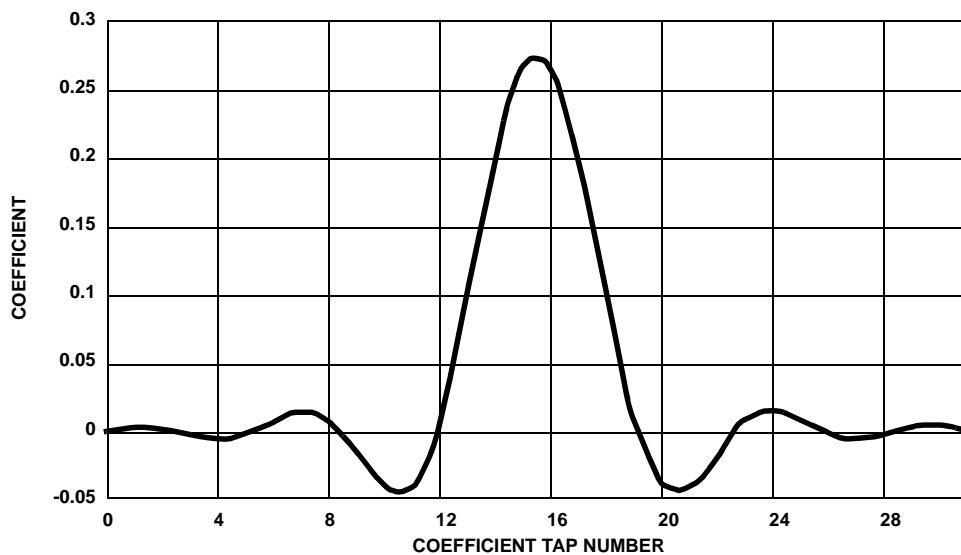

FIGURE 8. COEFFICIENTS FOR THE b128fir.cfg CONFIGURATION FILE FILTER: rrc4a4x.imp

The final field of the file name is the filter type. The options are RRC for Square Root of Raised Cosine α = 0.4 filtering (for bandlimited applications), I&D for Integrate and Dump filtering (for unfiltered data applications), and FIR filtering (for creating application specific onboard serial FIR filters). Figure 7 details the coefficients of the RRC Cosine α = 0.4 filter. The FIR selection implies that the DCL RCC and I&D filters are bypassed. In this case the file represents the coefficients for the FIR filter. Figure 8 details the coefficients for the FIR filter in example configuration file. Table 1 lists the configuration files provided as examples with the EVAL Kit and details the modulation format, data rate and filtering associated with each file.

When using the "fir" filter configuration, the FIR filter coefficient file that is used can be changed. Figure 8 illustrates that the Data Path/Modulation Menu Item (14) must be

selected and changed from "0" (Bypassed) to "1" (Enabled). After selecting "1", the user is prompted for the file name of the filter. The software will automatically append a ".rpt" suffix to the file name, indicating a SERINADE generated file, so do not enter a suffix with your file name. A number of example FIR filter files have been included on the distribution disk in the kit under the **FILTERS** directory, for the evaluation of a variety of Square Root of Raised Cosine filters. The files with the "**.imp**" suffix are files ready to import into **SERINADE**. The **SERINADE** FIR filter design software is included on the Evaluation Kit Distribution Disk, allowing the user to create files for specific applications. The files with the "**.rpt**" and "**.ser**" suffixes are generated by **SERINADE**. The HSP50110/210EVAL software uses the files with the "**.rpt**" suffix. Table 2 defines the available FIR filter coefficient files.

HSP50110/210 Evaluation Board Software

DATA PATH/MODULATION MENU

```
Current File Name.\B128RRC
(1) Master Clock Freq. . . . . . . . . . . . . . . . . . 40000000Hz
(2) Input Sample Rate . . . . . . . . . . . . . . . . . 40000000Hz
(3) Input Mode . . . . . . . . . . . . . . . . . . . . . . . . . . . Gated
(4) DQT Input Samples . . . . . . . . . . . . . . . . . . . . . .Real
(5) DQT Input Format. . . . . . . . . . . . . . . . . . . Offset Bin
(6) L.O. Center Freq. . . . . . . . . . . . . . . . . . .+5000000 Hz
(7) Data Modulation . . . . . . . . . . . . . . . . . . . . . . . BPSK
(8) Baud Rate. . . . . . . . . . . . . . . . . . . . . . . . . 128000Hz
(9) DQT Output Rate . . . . . . . . . . . . . . . . . . . 256000Hz
(10) I.F. NBW . . . . . . . . . . . . . . . . . . . . . . . . . . 750000Hz
(11) DQT Filter . . . . . . . . . . . . . . . . . . . . . . . CIC w/Comp
(12) DCL RRC Filter. . . . . . . . . . . . . . . . . . . . . .Enabled
(13) DCL I&D . . . . . . . . . . . . . . . . . . . . . . . . . . Bypassed
(14) HSP43124 . . . . . . . . . . . . . . . . . . . . . . . .Bypassed
(15) Es/No (min). . . . . . . . . . . . . . . . . . . . . . . . . . .+0dB
(16) Es/No (max. . . . . . . . . . . . . . . . . . . . . . . . .+100dB
(17) Es/No (design) . . . . . . . . . . . . . . . . . . . . . . . .+6dB
(18) A/D backoff (min.) . . . . . . . . . . . . . . . . . . . . 12dB
(19) A/D backoff (max.) . . . . . . . . . . . . . . . . . . . . 18dB
(20) DCL Output Vector . . . . . . . . . . . . . . . . . . -6dBFS
(21) DQT Output Level. . . . . . . . . . . . . . . . . . . -12dBFS
(22) DCL Detect. Level. . . . . . . . . . . . . . . . . . . -12dBFS
(23) Slicer Threshold . . . . . . . . . . . . . . . . . . . . . . 0.25
(24) DQT AGC Slew Rate . . . . . . . . . . . . . . . 30dB/sec
(25) DCL AGC Slew Rate . . . . . . . . . . . . . . . .10dB/sec
(26) AGC Limits . . . . . . . . . . . . . . . . . . . . . . FULL RANGE
(27) Output Mux Control. . . . . . . . . . . . . . . . . . . . . . 7
(0) MAIN MENU
ENTER SELECTION: (14) ⟵
```

FIGURE 9. DATA PATH/MODULATION MENU ITEM (14) IS USED TO SELECT THE ONBOARD SERIAL FIR FILTERS

TABLE 1. EXAMPLE CONFIGURATION FILE DEFINITIONS

NO.	FILE NAME	MODULATION FORMAT	SYMBOL RATE (KSps)	DATA RATE (KBps)	FILTER TYPE
1	b1024rrc.cfg	BPSK	1024	1024	Square Root of Raised Cosine
2	b128fir.cfg	BPSK	128	128	Serial FIR
3	b128i&d.cfg	BPSK	128	128	Integrate and Dump
4	b128rrc.cfg	BPSK	128	128	Square Root of Raised Cosine
5	b19p2i&d.cfg	BPSK	19.2	19.2	Integrate and Dump
6	b1p23i&d.cfg	BPSK	1.23	1.23	Integrate and Dump
7	b1p2i&d.cfg	BPSK	1.2	1.2	Integrate and Dump
8	b256rrc.cfg	BPSK	256	256	Square Root of Raised Cosine
9	b2.4i&d.cfg	BPSK	2.4	2.4	Integrate and Dump
10	b32i&d.cfg	BPSK	32	32	Integrate and Dump
11	b32rrc.cfg	BPSK	32	32	Square Root of Raised Cosine
12	b4p8i&d.cfg	BPSK	4.8	4.8	Integrate and Dump
13	b512rrc.cfg	BPSK	512	512	Square Root of Raised Cosine
14	b64i&d.cfg	BPSK	64	64	Integrate and Dump
15	b64rrc.cfg	BPSK	64	64	Square Root of Raised Cosine
16	b9p6i&d.cfg	BPSK	9.6	9.6	Integrate and Dump
17	q1024rrc.cfg	QPSK	1024	2048	Square Root of Raised Cosine
18	q128i&d.cfg	QPSK	128	256	Integrate and Dump
19	q128rrc.cfg	QPSK	128	256	Square Root of Raised Cosine
20	q1544rrc.cfg	QPSK	1544	3088	Square Root of Raised Cosine
21	q2048rrc.cfg	QPSK	2048	4096	Square Root of Raised Cosine
22	q256rrc.cfg	QPSK	256	512	Square Root of Raised Cosine
23	q32i&d.cfg	QPSK	32	64	Integrate and Dump
24	q32rrc.cfg	QPSK	32	64	Square Root of Raised Cosine
25	q512rrc.cfg	QPSK	512	1024	Square Root of Raised Cosine
26	q64i&d.cfg	QPSK	64	128	Integrate and Dump

TABLE 2. EXAMPLE FIR FILTER COEFFICIENT FILES

NO.	FILE NAME	SQUARE ROOT OF RAISED COSINE FILTER α	NUMBER OF TAPS	FILTER SPAN (SYMBOLS)	FILTER DECIMATION	REQUIRED DQT OUTPUT RATE
1	rrc2a2x	0.2	16	8	None	2 x Symbol Rate
2	rrc2a4x	0.2	32	8	2	4 x Symbol Rate
3	rrc2a8x	0.2	64	8	4	8 x Symbol Rate
4	rrc35a2x	0.35	16	8	None	2 x Symbol Rate
5	rrc35a4x	0.35	32	8	2	4 x Symbol Rate
6	rrc35a8x	0.35	64	8	4	8 x Symbol Rate
7	rrc4a2x	0.4	16	8	None	2 x Symbol Rate
8	rrc4a4x	0.4	32	8	2	4 x Symbol Rate
9	rrc4a8x	0.4	64	8	4	8 x Symbol Rate
10	rrc5a2x	0.5	16	8	None	2 x Symbol Rate
11	rrc5a4x	0.5	32	8	2	4 x Symbol Rate

Summary

The HSP50110/210EVAL Kit includes software that enables the user to configure the hardware for data processing. Example configuration files represent a variety of symbol rates, filtering and modulation formats. Additional files are provided for using the onboard serial FIR filters. The following recommendations will facilitate your use of the HSP50110/210EVAL Kit:

1. It is recommended that users conform to the conventions used for naming both the configuration and FIR Filter Files, minimizing confusion when seeking application assistance.

2. It is critical that the user understand that the Evaluation Board outputs data at symbol rate, not the data rate. Setup problems masked when operating in the BPSK format, come to confuse the operator when higher level modulation formats are invoked. Review of the material on the first section of this Application Note can avoid the most common mistakes in modulator and demodulator test setups. QPSK and 8PSK modulators are likely to input data at the data rate, rather than the symbol rate, especially if the units have integral encoders. The HSP50110/210EVAL outputs I and Q data at the symbol rate, not the data rate. External generation of 2X or 3X clocks may be required to re-multiplex the data into a single data stream if decoding is not employed. Decoders generally require the I and Q symbols to properly perform decoding.

3. It is also recommended that users begin with one of the example configurations, rather than attempt an original configuration creation. The user needs to become familiar with the operation of the Evaluation Board before attempting the process of configuration design.

4. Users that wish to design application specific FIR filters should begin with the FIR configuration example. The second step should be to select a different FIR filter file for the example configuration. The third step is to use SERINADE to create an application specific FIR file. Following these steps will introduce the user to the operation of the Evaluation Board, the example configuration files, the example filter files and the SERINADE filter design software in a methodical order, minimizing confusion and reducing the likelihood of mistakes.

In standard Bit Error Rate Testers (BERT), maximal length sequences are used as the PseudoRandom test sequences. Common code lengths are 2^7-1, 2^{10}-1, 2^{15}-1, and 2^{23}-1. One of the properties of these codes is that if every other bit of the sequence is selected, the original sequence will be generated at the lower rate at a new phase of the code. This property can be useful when testing the card in the QPSK mode when regeneration of the composite data rate cannot be done. The receive BERT should be set to the same code length as the transmit BERT but the symbol rate is entered as the operating rate. Either I or Q is connected to the BERT. Bit Error Rate data can be taken at the symbol rate. Note that imperfections in implementing the modulator (I/Q imbalance, d.c. offset, orthogonality, etc.) may degrade the BER of the individual channels (I or Q) at one or more of the lock points. Ideally, the BER at each lock point (2 for BPSK, 4 for QPSK, and 8 for 8PSK) will be identical. By taking an average of the BER on the I and Q Channels at the various lock points, the composite I/Q BER can be calculated.

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